## Amendments to the Specification

- Please replace the paragraph beginning at page 11, line 4, with the following amended paragraph:

The programmable logic device 64 also outputs signals to an open collector driver 108 which, in turn, forwards an ultrasound activation inhibit signal 110 to an ultrasound activation inhibit output 112. Another output to an inverting buffer 114 supplies a multiple probe controller ready signal output 116, which becomes true (on, sinking current) when control changes can be accepted and false (off, open) when control changes will be ignored. Thus, a disconnected cable sends a not ready (false) signal to the ~~multiple probe~~ automation controller.

- Please replace the paragraph beginning at page 18, line 1, with the following amended paragraph:

The use of synchronous digital logic eliminates nearly all the timing requirements that the automation control system 24 must observe. According to some embodiments, the only timing requirement is that the probe selection must occur (when the multiple probe controller 14 is ready) at least a set time—for example, 40 ms—before ultrasound power is activated. The synchronous logic of the multiple probe controller 14 does introduce some timing uncertainty ~~occurring~~ that occurs with the external ultrasound activation signal, which is asynchronous to the internal logic in some embodiments. Using an internal (integrated) weld timer will allow for synchronized logics and eliminate this timing uncertainty.